

FIG. 1

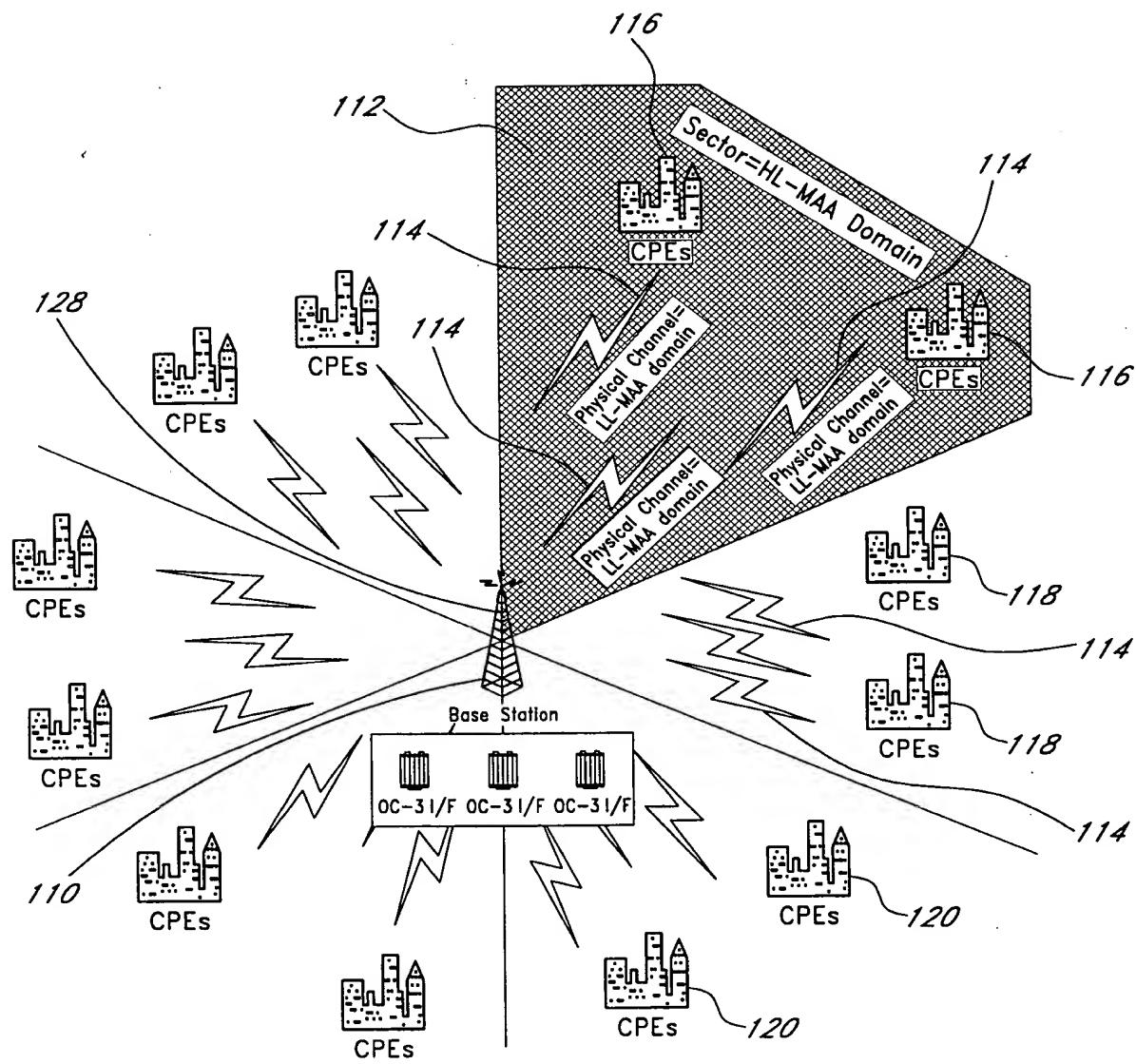
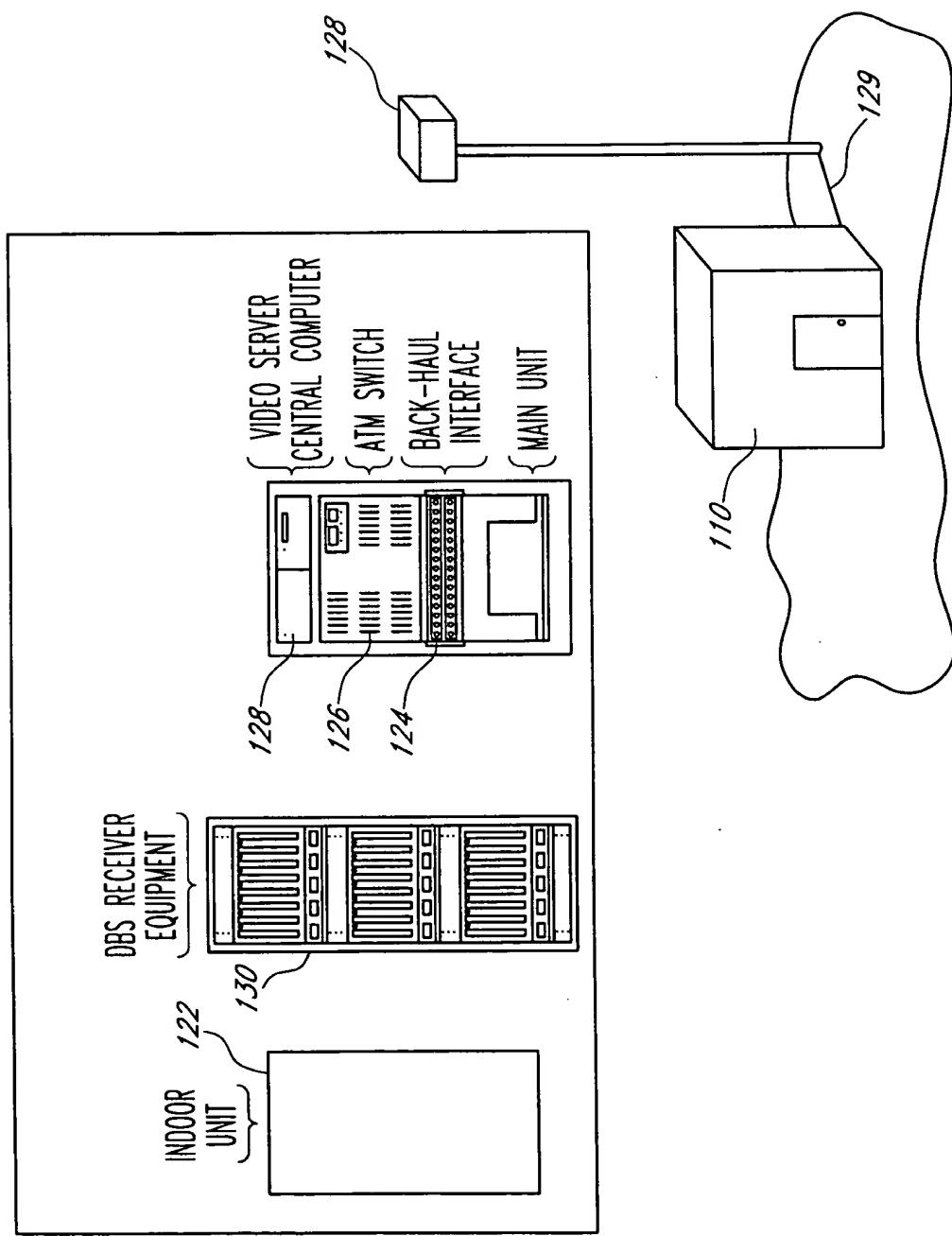
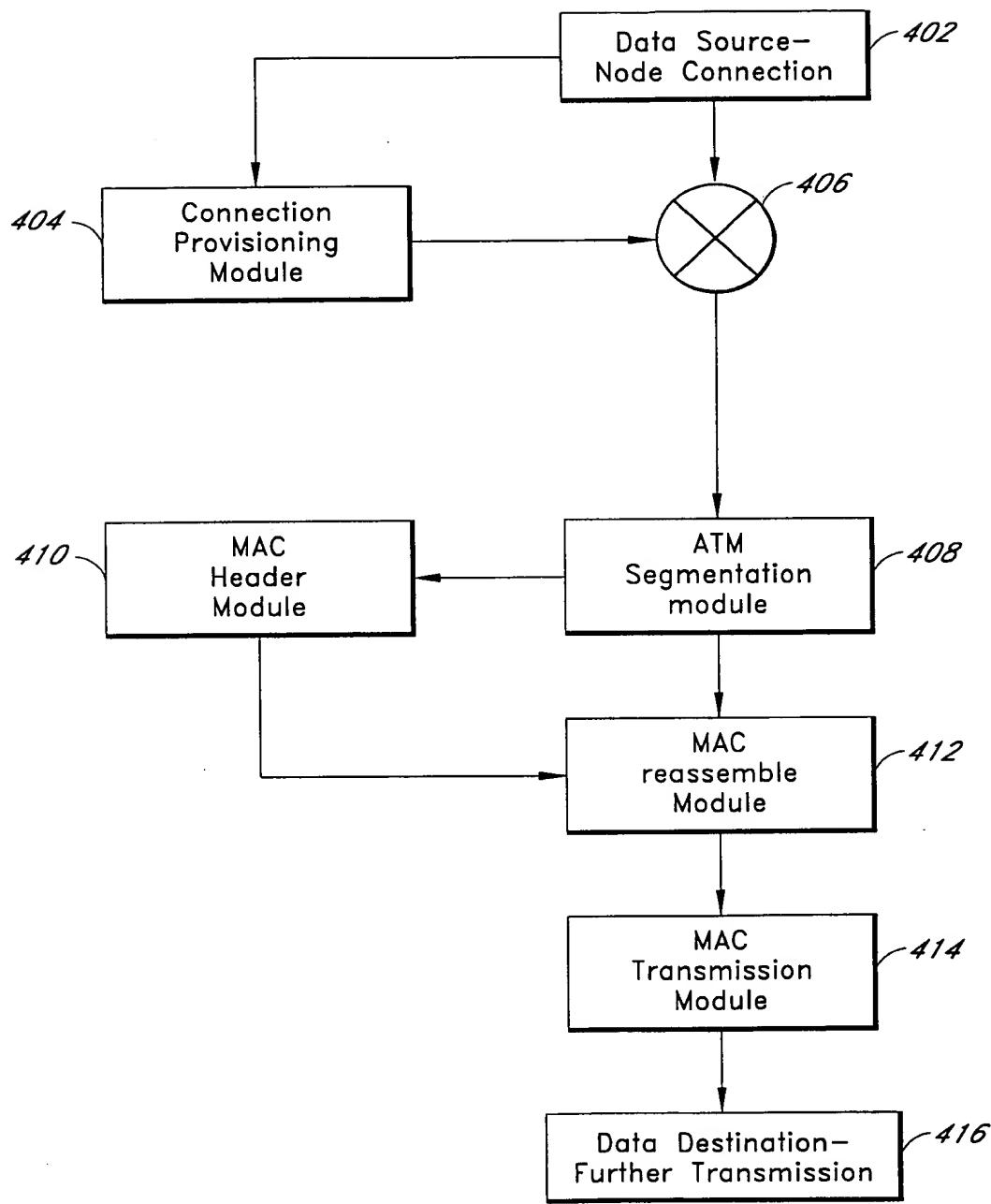
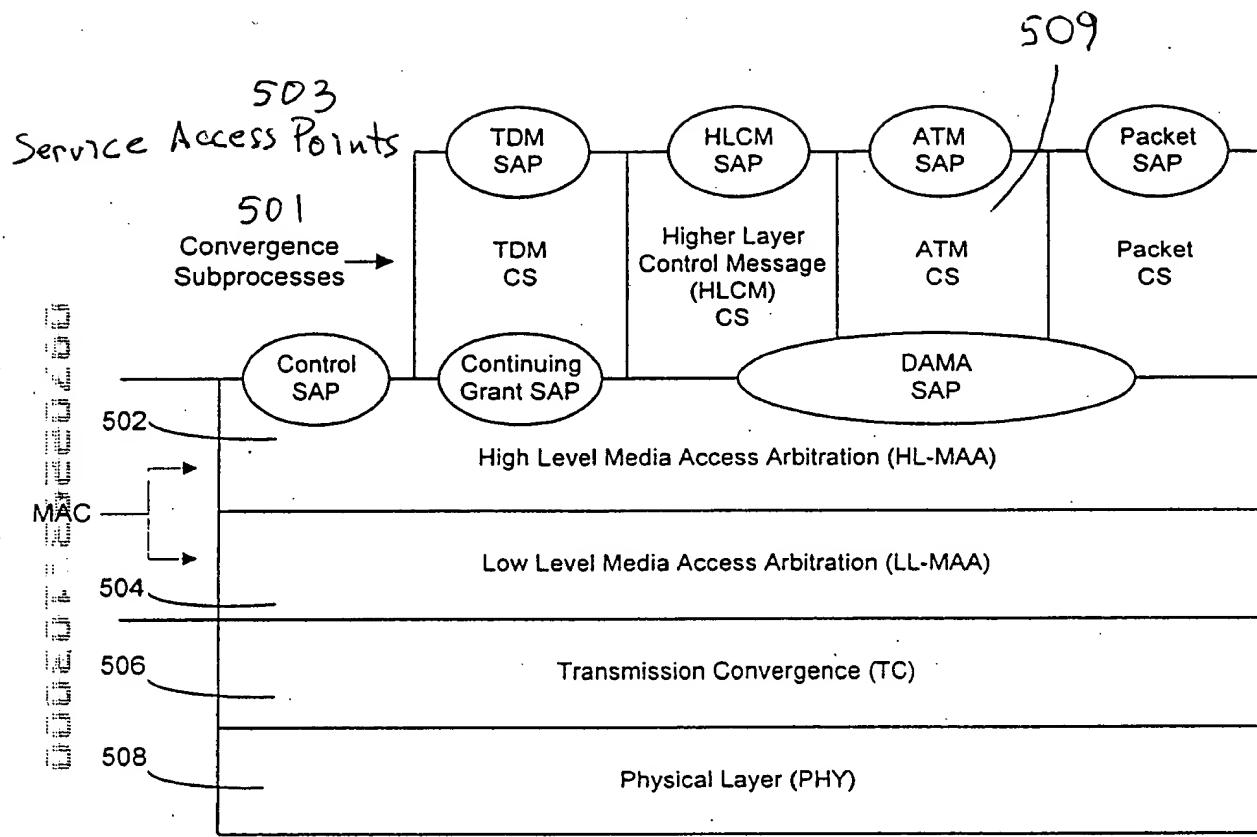


FIG. 2

FIG. 3







Layered Data Transport Architecture

FIG. 5

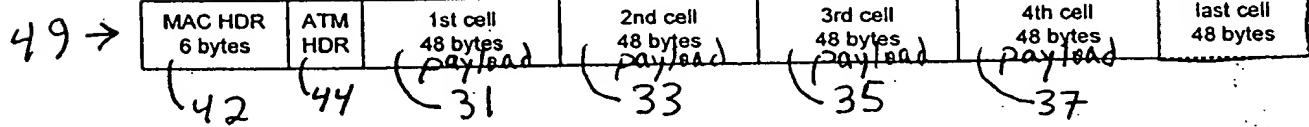
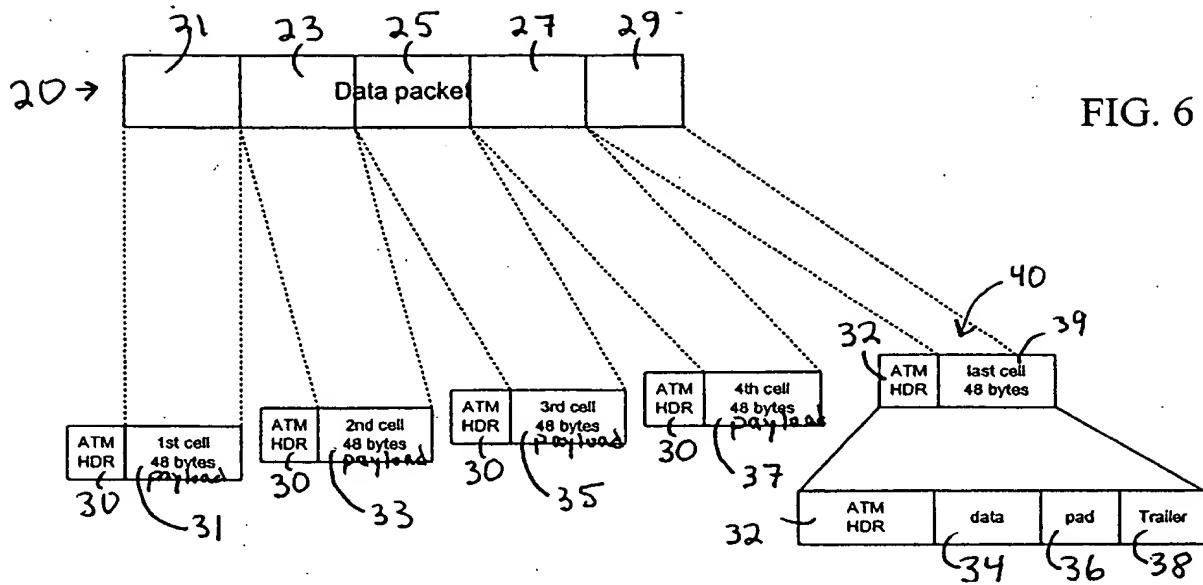


FIG. 7

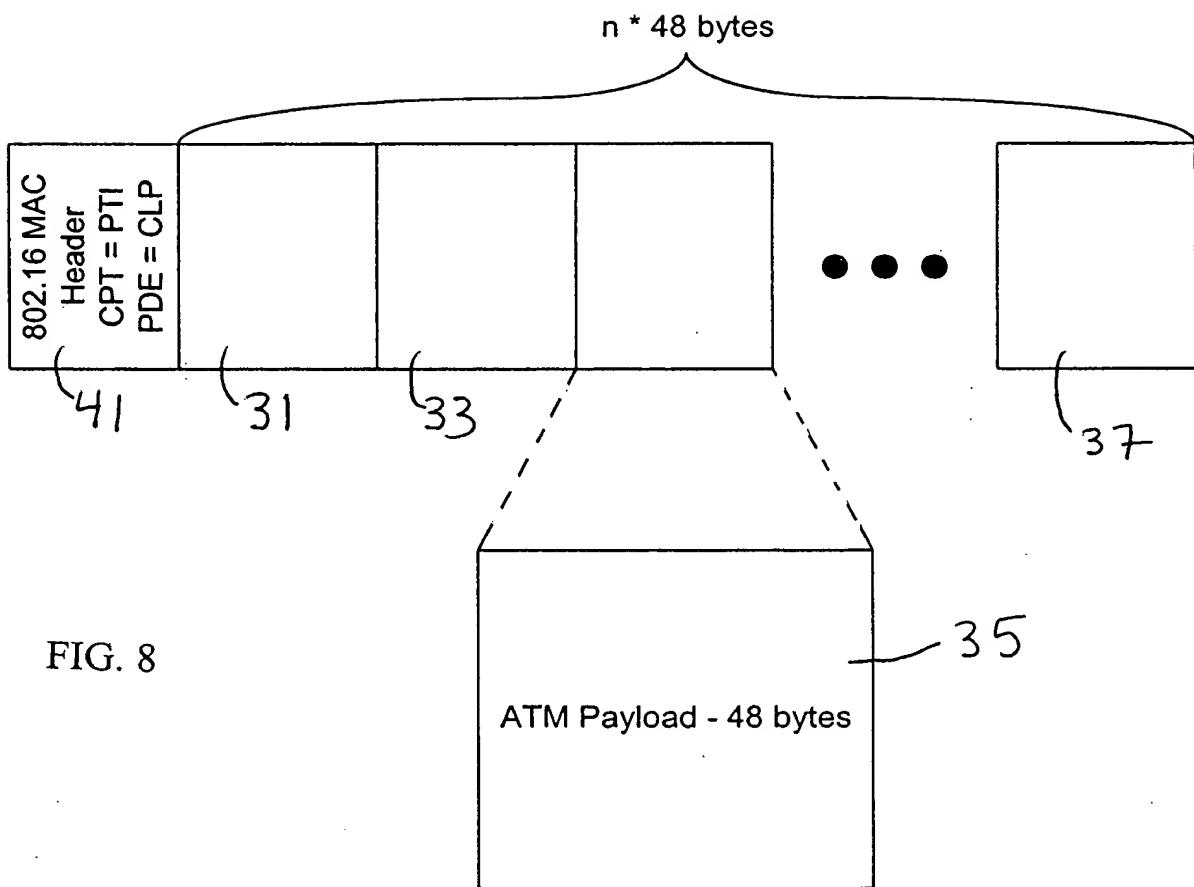


FIG. 8

FIG. 9

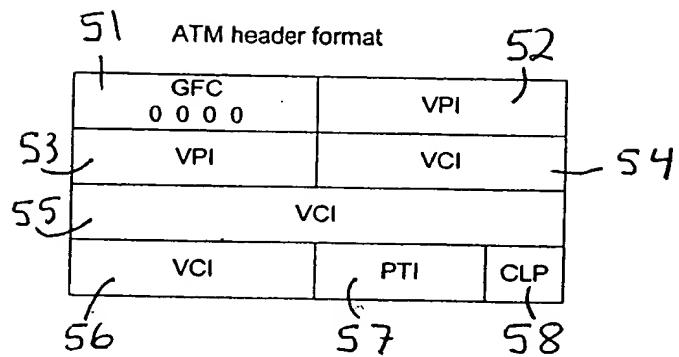
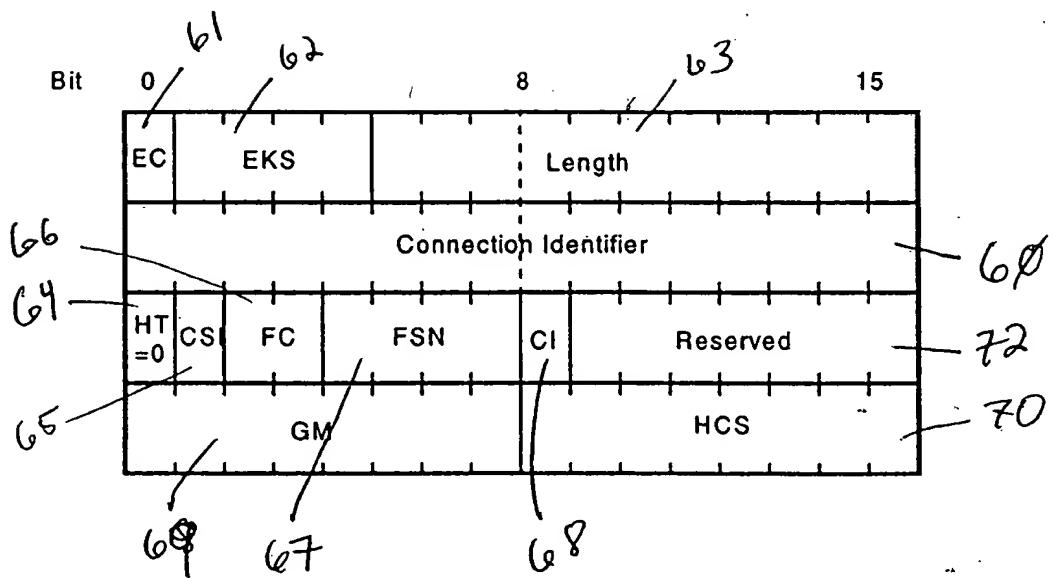


FIG. 10



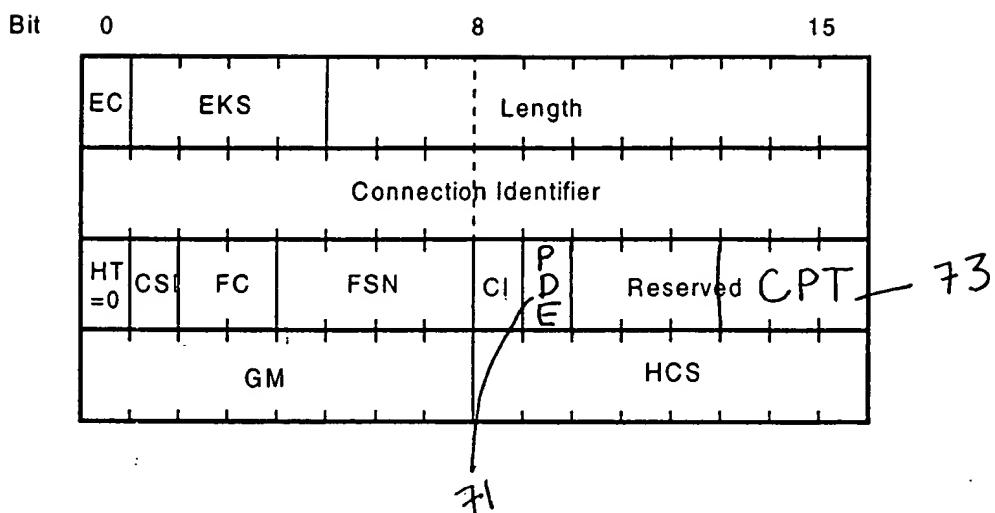


FIG. 11

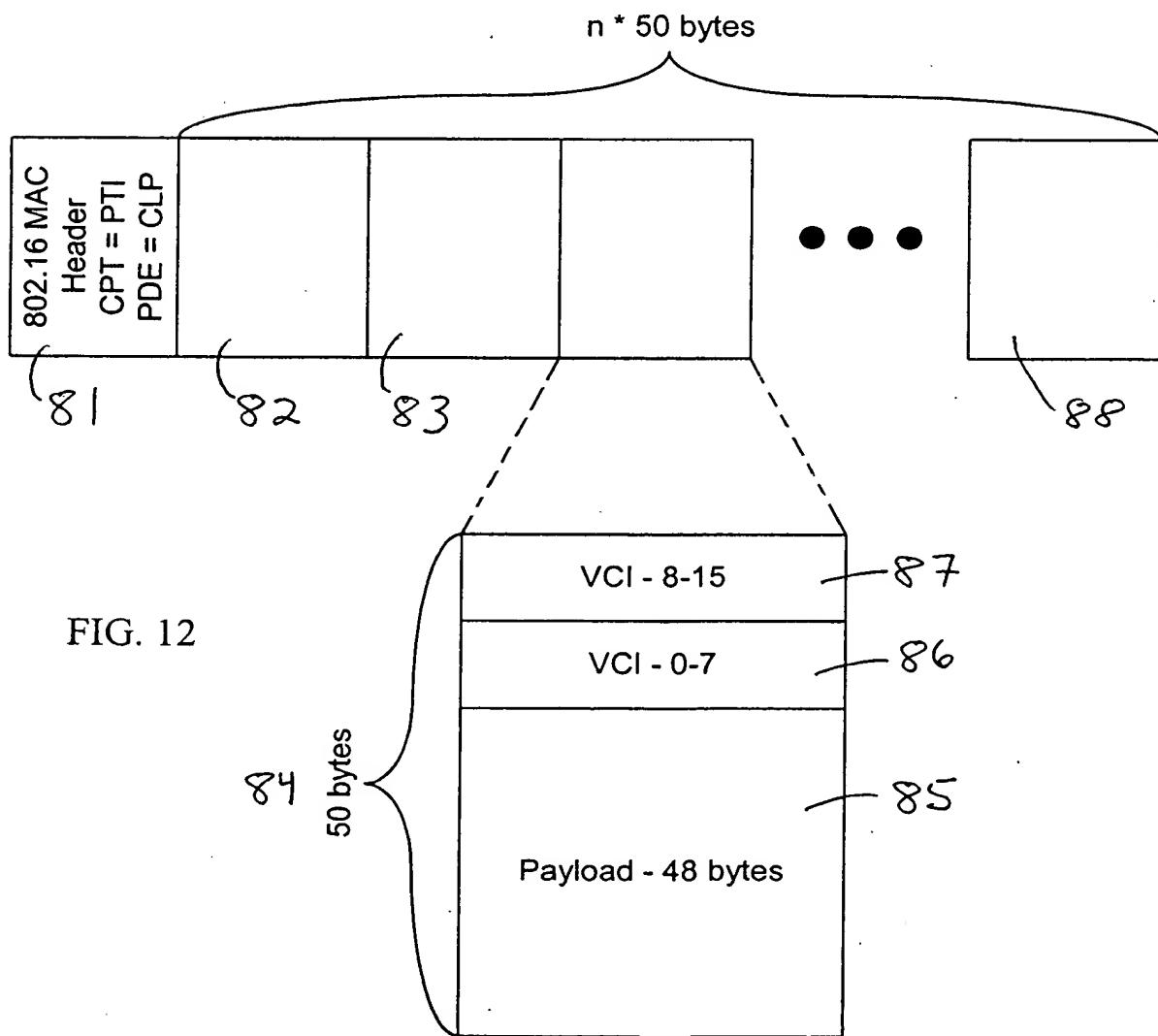


FIG. 12

91

MAC header format

EH 1	PC/PM	CIDa
CIDa	CIDb	
CIDb		
CIDb	CPT	PDE
Length		

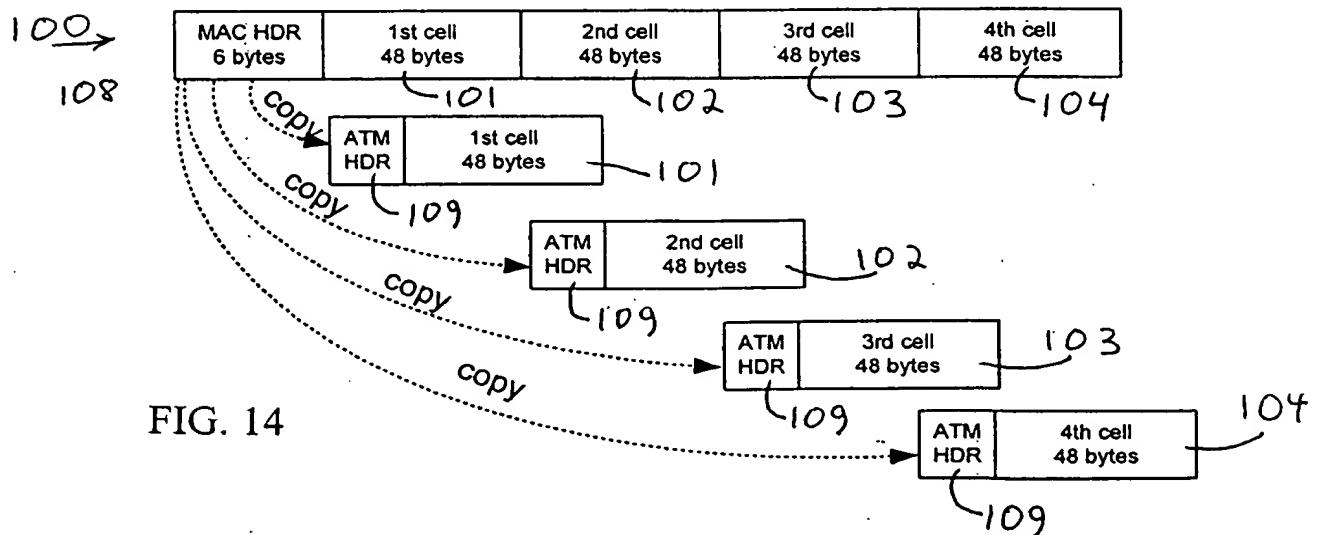
ATM header format

GFC 0 0 0 0	VPI	
VPI	VCI	
VCI		
VCI	PTI	CLP

FIG. 13

Mapping:

MAC header	ATM header
EH/PC/PM	GFC (set to zero at the northbound interface between the ATM and MAC)
CIDa	VPI
CIDb	VCI
CPT	PTI
PDE	CLP
Length	N/A no need to map.



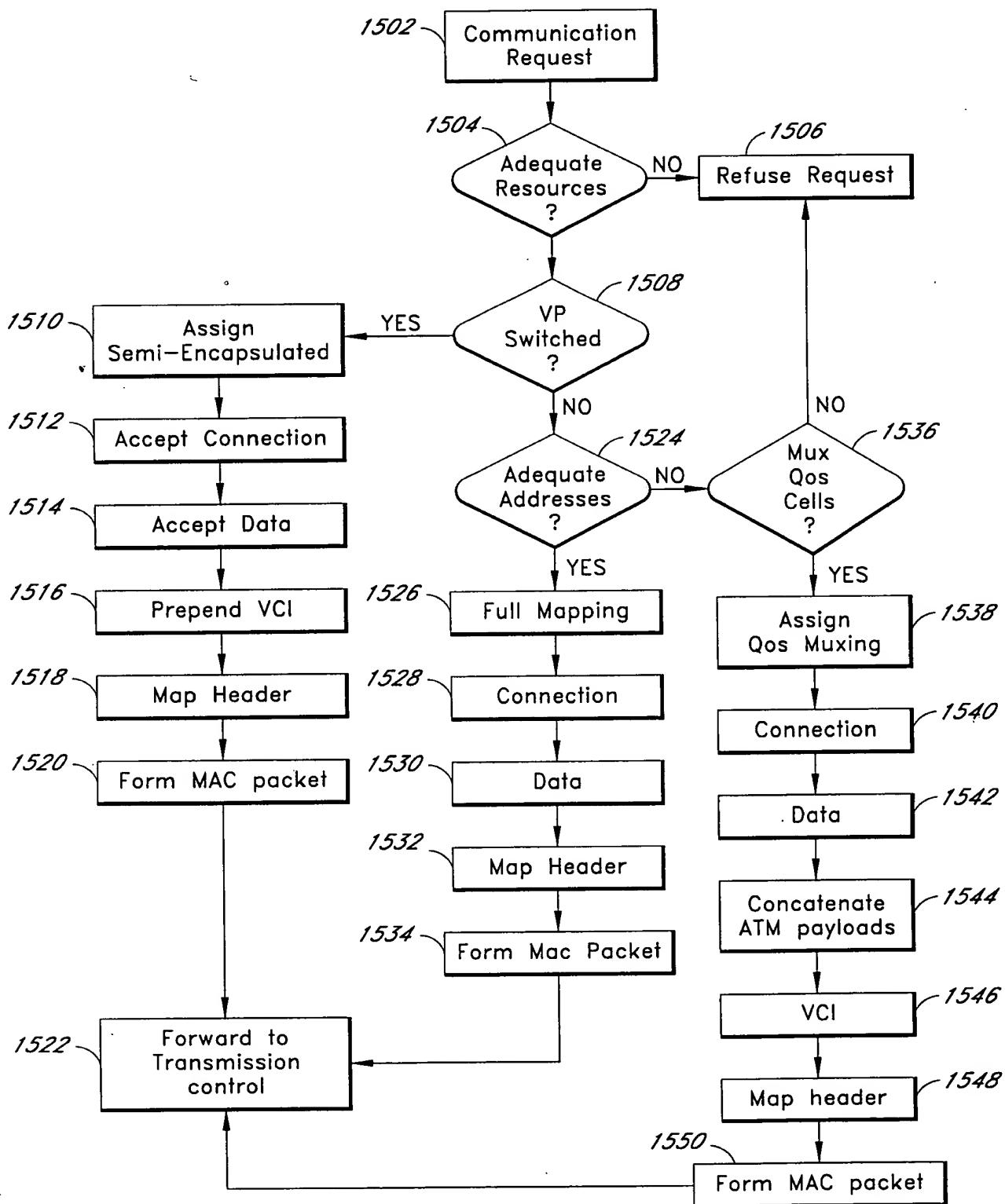


FIG. 15